Electronic Version
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Claims

[c1] 1.A wafer acceptance testing (WAT) method for monitoring gate conductor-deep trench (GC-DT) misalignment, comprising the steps of:
providing a test key structure comprising a deep trench capacitor structure biased to a first voltage (V_{DT}) embedded in a substrate, an active area being defined on the substrate, wherein the deep trench capacitor structure is electrically connected to an out diffusion in the active area and is isolated by shallow trench isolation (STI), and the deep trench capacitor structure comprises interdigitated GC-T electrode layout and GC-B electrode layout, wherein the GC-T electrode layout is biased to a second voltage (V_{GC-T}), and the GC-B electrode layout is biased to a third voltage (V_{GC-B}), and wherein the GC-T electrode layout comprises a plurality of first GC fingers, the GC-B electrode layout comprises a plurality of second GC fingers;
measuring a capacitance of a first capacitor C1, wherein the GC-T electrode layout serves as a first electrode of the first capacitor C1 and the out diffusion serves as a second electrode of the first capacitor C1;
measuring a capacitance of a second capacitor C2,

wherein the GC-B electrode layout serves as a first electrode of the second capacitor C2 and the out diffusion serves as a second electrode of the second capacitor C2; and

comparing the capacitance of the first capacitor C1 with the capacitance of the second capacitor C2, wherein if $C_1 \neq C_2$, GC-DT misalignment occurs.

[c2] 2.The WAT method according to claim 1 wherein the second voltage (V_{GC-T}) equals to the third voltage (V_{GC-B}).

[c3] 3. The WAT method according to claim 1 wherein the deep trench capacitor structure further comprises a buried plate disposed in the substrate adjacent to a lower portion of the deep trench capacitor structure, a storage node, and a capacitor dielectric disposed between the storage node and the buried plate, wherein the storage node is electrically connected to the out diffusion.

[c4] 4.The WAT method according to claim 1 wherein the GC-T electrode layout comprises a first bridge portion for electrically connecting the plurality of first GC fingers with a first contact portion.

[c5] 5.The WAT method according to claim 1 wherein the GC-B electrode layout comprises a second bridge portion for

electrically connecting the plurality of second GC fingers with a second contact portion.

[c6] 6.A test key structure for monitoring gate conductor-deep trench (GC-DT) misalignment, comprising:
a deep trench capacitor structure biased to a first voltage (V_{DT}), wherein the deep trench capacitor structure is embedded in a substrate and comprises an out diffusion formed in an active area of the substrate, and wherein the deep trench capacitor structure is isolated by shallow trench isolation (STI);
an insulation layer formed on the active area;
a GC-T electrode layout biased to a second voltage (V_{GC-T}), the GC-T electrode layout comprising a plurality of first GC fingers; and
a GC-B electrode layout biased to a third voltage (V_{GC-B}), the GC-B electrode layout comprising a plurality of second GC fingers, wherein the first GC fingers and the out diffusion constitute a first capacitor C1, and the second GC fingers and the out diffusion constitute a second capacitor C2, and wherein the first GC fingers and the second GC fingers are interdigitated.

[c7] 7.The test key structure according to claim 6 wherein there is no source/drain ion doped region implanted into the substrate between two adjacent GC fingers.

[c8] 8.The test key structure according to claim 6 wherein the GC-T electrode layout comprises a first bridge portion for electrically connecting the plurality of first GC fingers with a first contact portion.

[c9] 9.The test key structure according to claim 6 wherein the GC-B electrode layout comprises a second bridge portion for electrically connecting the plurality of second GC fingers with a second contact portion.